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EXAMINER	
HO, THOMAS M	

ART UNIT	PAPER NUMBER
2132	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/672,367	MCKEEN ET AL.	
	Examiner	Art Unit	
	Thomas M. Ho	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/21/07

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. ***The amendment of 2/21/07 has been received and entered.***

2. ***Claims 1-12, 14-22 are pending.***

Response to Amendments

The Applicant has argued:

Page 6:

England discloses a software structure for protecting premium content using code modules that are arranged in a hierarchy of trust (Abstract and FIG. 4). However, England does not disclose a graphics card that can access different areas of the system memory according to an access mode asserted by the graphics card. Rather, England discloses that peripheral devices (e.g., a sound card) are granted access to the system memory according to their physical locations in the PCI (or other expansion bus) slot (col. 13, lines 19-27). Granting access by physical slot locations is entirely different from granting access according to an access mode asserted by the peripheral device. In England, once a sound card is placed into a PCI slot, the region of system memory to which it has access is determined. To access a different region of the system memory, the sound card needs to be plugged into a different PCI slot that is conferred a different level of trust. The same sound card cannot actively assert one access mode to access one area of the

system memory and assert another access mode to access another area of the system memory. Thus, England does not disclose that the system memory is accessible according to an access mode asserted by the graphics card.

The Examiner has considered the Applicant's arguments, but has found them to be unpersuasive. The Examiner notes specifically in claim 1 that the Applicant recites a normal execution mode, and an isolated execution mode but then recites the third term "access modes" with reference to the graphics card. However it is the Examiner's position that the recitation of the term "access mode" is sufficiently broad as to construe any manner of memory access. That is to say, any application or hardware piece that seeks to access memory may be broadly construed to be performing access according to an "access mode." Even a sound card that seeks to access memory to write recorded audio to a memory, or read audio to be played from a memory may be construed to be accessing memory in different "access modes"—in this particular case, a read mode and write mode.

Pages 6-7:

With respect to Claim 12, this claim is amended to include the element of "handling the output data from the isolated output area and non-isolated area of the system memory differently at a graphics card that operates, and has different memory access privileges, in a normal execution mode and the isolated execution mode." England does not disclose these elements. England does not disclose a graphics card that operates in two different execution modes.

England also does not disclose a graphics card that has different memory access privileges in two different execution modes. Moreover, England does not disclose that a graphics card handles the output data from the isolated output area and non-isolated area of the system memory differently. As mentioned above in regard to Claim 1, England at most discloses that a sound card can access a specific region of memory according to its physical slot location. Thus, England does not teach or suggest each of the elements of amended Claim 12.

England (Column 7, lines 65 – Column 8, line 64) reveals a method in which trust is extended to the graphics card software.

England discloses four different trust levels within his invention each of which ensures its trust level based on a secure access of memory. These levels, A,B,C,D are illustrated in Figure 2, and (Column 5, lines 35 – Column 6, line 32) Each of these security levels has associated with it a specific memory. For Example, the area of memory accessible by level C applications is known as Ring C memory. (Column 6, lines 1-5)

Applicant's contention with Claim 12 appears to be that England does not disclose a graphics card that operates in two different execution modes.

The Examiner contends that the extension of trust provided by the secure content provide module on (Column 8, lines 20-35 and its equivalent diagram in Figure 4) to the audio-card driver

module discloses the graphics card handling access to memory in at least two levels of access control.

Page 7:

With respect to Claim 17, England does not teach or suggest "occluding all windows but the first window." Applicants have carefully reviewed the cited passage and the disclosure in general but have been unable to identify any part of the disclosure that mentions occluding windows. Applicants request that the Examiner point out the specific location of such teaching in the disclosure. Accordingly, reconsideration and withdrawal of the § 103 rejection of Claims 245, 7-11, 14 and 17 are requested.

The Examiner notes that it was for this deficiency that Cunnif was raised as additional art for a § 103 rejection.

Page 8:

Cunnif does not cure the deficiencies of England. Cunnif is relied on for disclosing image occlusion. However, Cunnif does not disclose "a graphics card coupled to the processor and accessible to different areas of the system memory according to access modes asserted by the graphics card," as claimed in base Claim 12. Thus, England in view of Cunnif does not teach or suggest each of the elements of Claims 17 and 18.

This portion of Applicant's argument is addressed above in reference to the arguments and the rejection of claim 12.

Page 8:

Moreover, with respect to Claim 17, the Examiner indicates that Cunnif discloses occluding all objects behind a bounding box, which is created to enclose the primitives within that object (Office Action on page 16, lines 3-4). However, "all objects behind a bounding box" is different from "all windows on a display." Cunnif at most discloses that the objects behind the bounding box are occluded. Cunnif does not mention whether other displayed objects, which are not behind the bounding box, are occluded. Thus, England in view of Cunnif does not teach or suggest each of the elements of Claim 17 for this additional reason.

This portion of Applicant's arguments are addressed in reference to the changes to the rejection below made in light of Applicant's amendments to the claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites "wherein local storage of the data in the graphics card...is not permitted"

This could be reasonably interpreted as:

1) Not permitting the writing of data to the graphics card memory. (the graphics card local storage)

2) Not permitting the contents of the data stored within the graphics card memory to be stored within regular system memory(including isolated/secure memory).

For purposes of examination, interpretation 2 has been construed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 6, 12, 13, 15, 16, 19-22 rejected under 35 U.S.C. 102(e) as being anticipated by England et al., US patent 6775779.

In reference to claim 1:

England et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution mode, where the processor can execute in different modes and the isolated execution mode is the secure mode of execution and where the secure modes of execution comprise four modes, A,B,C,D ,each with a varying degree of isolatedness in its execution security (Column 5, lines 35-55) & (Column 5,lines 65 – Column 6, line 25)
- A system memory accessible to the processor(Column 5, lines 5-35) & (Figure 1, Item 140, 141) including an isolated area, an isolated output area, and a non-isolated area,

where the system memory is divided into rings of isolation or protection, and these memory areas are one of the means by which the processor executes in isolated execution mode. (Figure 2) & (Column 5, line 55 – Column 6, line 12)

- A graphics card coupled to the processor and accessible to different areas of the system memory according to access modes asserted by the graphics card, where the output device is an I/O adaptor that may be a monitor, video card frame buffer or sound card, and where the output device is coupled to the processor in that the output devices receive processed information from the processor. (Figure 1, Item 170, 172) & (Column 4, line 40-55) & (Column 13, lines 1-50) , and where the trust is transferred to the graphics card drivers and applications to allow trusted access in an isolated mode of execution & (Column 7, line 55) – (Column 8, line 53) or a regular mode of execution (Ring D, (Column 5,lines 65 – Column 6, line 25))

In reference to claim 6:

England et al. discloses the platform of claim 1 further comprising:

- An operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in the isolated execution mode, where the operating system provides a secure operating environment and wherein the secure mode involves input/output conversions. (column 5, lines 13-35)

In reference to claim 12:

England et al discloses a method comprising: (Column 7, lines 50-56) & (Column 12, line 25-Column 13, line 50) & (Column 8, line 25-52)

- Establishing an isolated execution environment having an isolated execution mode by providing hardware support for the isolated execution mode, where the isolated execution environment is an secure execution mode, where the hardware support for the isolated execution mode is provided in the Access control table of (Figure 3), further described in (Column 6, lines 45-50) & (Column 6, line 65 – Column 7, line 5) The access control table is a hardware circuit, in particular a memory(Column 6, lines 33-35) whose information causes the gates to pass or block processor read/write controls.
- Preventing access to output data in an isolated output area of a systems memory by any requester not operating in an isolated mode, where the output area where output data is written to is protected from external modification or access. where the isolated attribute is a CC code attached to requests to indicate it is part of the secure operating mode. And Denying the request if no isolated attribute is present, (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52) where the attribute is denied if no CC code is found, or it is improper.
- Handling the output data from the isolated output area and non-isolated area of the system memory differently at a graphics card that operates, and has different memory access priviledges in a normal execution mode and the isolated execution mode, where the trust is transferred to the graphics card drivers and applications to allow trusted access

in an isolated mode of execution & (Column 7, line 55) – (Column 8, line 53) or a regular mode of execution (Ring D, (Column 5,lines 65 – Column 6, line 25))

In reference to claim 13:

England et al. discloses the method of claim 12 wherein establishing comprises:

- Segregating a system memory into an isolated output area and a non-isolated area. (Figure 2) & (Column 5, lines 55 – Column 6, line 32)

In reference to claim 15:

England et al. (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52) discloses the method of claim 12 wherein preventing comprises:

- Identifying if an isolated attribute is present in a request for access to the requested output area, where the isolated attribute is a CC code attached to requests to indicate it is part of the secure operating mode. And Denying the request if no isolated attribute is present, where the attribute is denied if no CC code is found, or it is improper.

In reference to claim 16:

England et al. (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52) discloses the method of claim 12 further comprising:

- Loading data from the isolated output area into a bit plane on the graphics card, where the bit plane is the frame buffer.
- Denying all external access to the bit plane, where external access is denied by unauthorized access attempts.

In reference to claim 19:

England et al. discloses a platform comprising:

- A processor executing in one of a normal execution mode and an isolated execution mode; (Column 5, lines 35-55)
    - The processor including an isolated execution circuit to provide hardware support for the isolated execution mode where the hardware support for the isolated execution mode is provided in the Access control table of (Figure 3), further described in (Column 6, lines 45-50) & (Column 6, line 65 – Column 7, line 5) The access control table is a hardware circuit, in particular a memory(Column 6, lines 33-35) whose information causes the gates to pass or block processor read/write controls.
- A direct memory access controller to issue requests for access to an isolated output area of a system memory that includes the isolated output area and a non-isolated area; (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52) & (Column 13, lines 35-50)

- A first interface coupled to the DMA controller to forward requests to a memory control hub (MCH); (Column 12, lines 25 – Column 13, line 50) & (Column 7, line 50-line 56) & (Column 8, line 25-52)
- A second graphics card coupled to the MCH controller to supply output data to an output device, the graphics card accessible to different areas of the system memory according to access modes asserted by the graphics card. (Figure 1, Item 171, 172) & (Column 4, lines 40-55), and where the trust is transferred to the graphics card drivers and applications to allow trusted access in an isolated mode of execution & (Column 7, line 55) – (Column 8, line 53) or a regular mode of execution (Ring D, (Column 5,lines 65 – Column 6, line 25))

In reference to claim 20:

England et al. discloses the apparatus of claim 19 wherein the first interface is a secure accelerated graphics port (AGP) and the output device is a display. (Column 4, lines 15-40)

In reference to claim 21:

England et al. discloses the apparatus of claim 19 wherein the DMA controller attaches an isolated attribute to any isolated output area access request, where the isolated attribute is a CC code. (Column 6, lines 19-65) & (Column 7, lines 50-56)

In reference to claim 22:

England et al. discloses the apparatus of claim 19 wherein the graphic card comprises logic to handle the output data from the isolated output area and the non-isolated area differently (Column 4, lines 40-55) & (Column 13, lines 20-50), and where the trust is transferred to the graphics card drivers and applications to allow trusted access in an isolated mode of execution & (Column 7, line 55) – (Column 8, line 53) or a regular mode of execution (Ring D, (Column 5,lines 65 – Column 6, line 25))

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-5, 7-11, 14, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over England et al. US patent 6775779.

In reference to claim 2:

England et al. fails to explicitly disclose the platform of claim 1, wherein the graphics card comprises logic to handle output data from the isolated output area and the non-isolated area differently.

England et al. discloses an embodiment where the trust is transferred to the graphics card drivers and applications to allow trusted access in an isolated mode of execution & (Column 7, line 55) – (Column 8, line 53) or a regular mode of execution (Ring D, (Column 5,lines 65 – Column 6, line 25)), where such trust is conferred based on a series of isolated modes of execution in four rings. (Column 5, line 65 – Column 6, line 25)

England et al. however teaches a method of protecting content through a method of secure processor modes combined with secure memories. (Abstract) & Figure 2)

England et al. additionally discloses that among this content, there may be audio and video content. It is further disclosed that access to these modules and drivers by requests external to the secure mode are restricted. (Column 2, lines 5-15) & (Column 2, line 65 – Column 3, line 10)

England et al. further discloses that the hardware components used may include that which is standard to a conventional PC. (Column 4, lines 15-40) and among the I/O devices that may serve as the isolated output area includes frame buffers. (Column 13, lines 1-50)

A search of the prior art has uncovered that PC frame buffers are frequently called graphics cards.

Framebuffer

From Wikipedia, the free encyclopedia

*(Redirected from **Frame buffer**)*

*Jump to: **navigation**, **search***

*The **framebuffer** is a video output device that drives a video display from a memory buffer containing a complete **frame** of data. The information in the buffer typically consists of color values for every **pixel** (point that can be displayed) on the screen. Color values are commonly stored in 1-bit **monochrome**, 4-bit **palletized**, 8-bit **palletized**, 16-bit **highcolor** and 24-bit **truecolor** formats. An additional **alpha channel** is sometimes used to retain information about pixel transparency. The total amount of the memory required to drive the framebuffer is dependent on the **resolution** of the output signal, as well as the **color depth** and **palette** size. Framebuffers differ significantly from the **vector graphics displays** that were common prior to the advent of the framebuffer. With a vector display, only the **vertices** of the graphics primitives are stored. The electron beam of the output display is then commanded to move from vertex to vertex, tracing an analog line across the area between these points. With a framebuffer, the electron beam (if the display technology uses one) is commanded to trace a left-to-right, top-to-bottom path across the entire screen, much in the same way a television renders a broadcast*

*signal. The color information for each point on the screen is then pulled from the framebuffer, creating a set of discrete picture elements (**pixels**).*

*(**PC** framebuffers are commonly referred to as "Graphics Cards"), many users assume that a framebuffer is simply an area of memory for storing graphics.*

Although England et al. does not explicitly recite the limitation of a graphics card, in light of the disclosures of the prior art, it would have been obvious to one of ordinary skill in the art to use graphics cards as part of the isolated output area, where the output of England et al. is written to (Column 13, lines 1-5) in order to preserve the security of secure system by regulating access to output data written to the video memory.

In reference to claim 3:

England et al. discloses the platform of claim 2 further comprising:

- A memory control hub (MCH) coupled between the system memory, and the processor and the graphics card, the memory control hub to permit the graphics card to access the isolated output area only when the graphics card is asserts an isolated access mode, where the directed memory controller in the Access control table is the Memory control Hub (Column 6, lines 45 – Column 7, line 5) which directs the processor regarding the specific modes of execution of the executing code. This in turn controls the processor

execution modes, and thus the output to the graphics cards where the graphics card is the video output adaptor with the frame buffer, and access to the frame buffer output is only permitted when in the secure mode. (Column 8, lines 25-53) & (Column 12, lines 25-67) & (Column 13, lines 1-18) & (Column 13, lines 37-50) & (Column 7, lines 50-55).

In reference to claim 4:

England et al. discloses the platform of claim 3 wherein the graphics card comprises:

- A direct memory access (DMA) controller and wherein local storage of the data in the graphics card from the isolated output area is not permitted, where attempts to transfer and store data from the output area to local storage such as memory is interdicted. (Column 7, lines 50-55) & (Column 13, lines 37-50)

In reference to claim 5:

England et al. discloses the platform of claim 3 wherein only the graphics card is permitted to read the isolated output area. (Column 12, lines 57-67) & (Column 13, lines 1-18) & (Column 10, lines 49-57)

In reference to claim 7:

England et al. discloses the platform of claim 3 further comprising:

A link between the graphics card and the MCH having an isolated transaction type, where the isolated transaction type is indicate by the secure CC number indication. (Column 12, lines 25-Column 13, line 15) & (Column 6, line 19-32)

In reference to claim 8:

England et al. discloses the platform of claim 3 wherein the MCH only permits the O/S nub to write to the isolated output area. (Column 12, line 25 – Column 13, line 50) & (Column 7, line 50-56) & (Column 8, line 25-52)

In reference to claim 9:

England et al. discloses the platform of claim 7 wherein the link is a secure accelerated graphics port bus, where the accelerated graphics port bus is an AGP port bus. (Column 4, line 15-40)

In reference to claim 10:

England et al. (column 6, lines 25-32) & (Column 12, line 25 – Column 13, line 50) discloses the platform of claim 2 wherein the graphics card comprises:

- An isolated bit plane for the output data from the isolated output area where the isolated bit plane is the memory of the frame buffer in secure more.
- A non-isolated for the output data from the non-isolated output area bit plane, where the non isolated bit plane is the memory of the frame buffer when in unprotected mode.

In reference to claim 11:

England et al. (Column 12, line 25 – Column 13, line 50) discloses the platform of claim 10 wherein the graphics card denies all external access to the isolated bit plane.

(Column 7, line 55) – (Column 8, line 53)

In reference to claim 14:

England et al. discloses the method of claim 12 further comprising:

- Issuing an isolated direct memory access (DMA) request for display data in the isolated output area from a graphics card; (Column 12, lines 25 – Column 13, line 50)
- Refreshing the display based on the display data, where refreshing to display based on the display data is inherent to the function and purpose of a frame buffer. (Column 13, lines 1-15)

8. Claims 17, 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over England et al. US patent 6775779 and Cunnif et al, US patent 6476806.

In reference to claim 17:

England et al. fails to disclose the method of claim 16 further comprising :

Defining a first window on an output display to present an image corresponding to the bit plane; and occluding all windows on the display but the first window.

Cunnif et al. (Column 2, lines 25-46) discloses a bounding box that is created to enclose all the primitives within that object. If it is determined that no pixels would be modified if the bounding box is rendered, then the objects behind the bounding box or "window" can be considered occluded.

Neither Cunnif nor England explicitly discloses that the bounding box would not have windows in front of it.

However, the Examiner takes official notice that "maximizing an application" such as the action performed in Windows style operating system was well known at the time of invention. In fact the Examiner is typing on a maximized Office application at the moment.

All current windows that are additionally open are occluded behind this single window. The option of maximizing a particular window on a screen allows a user to focus only on that application at the moment. Additionally, it saves the computer processing time, because the windows "behind" the maximized current window need not be rendered.

Cunnif et al. discloses that occluding an object that doesn't need to be rendered would decrease processing throughput. If computer user has open three windows, and currently one of them is maximized, then the graphical procsessing does not have to be performed in the other windows that are not currently displayed. It would have been obvious to one of ordinary skill in the art at

the time of invention to occlude all windows but the first window in order to decrease the processing throughput and increase the speed of the overall processing load.

In reference to claim 18:

England et al. discloses the method of claim 12 further comprising:

- Retrieving data from the isolated output area, where the value of the secure memory may be accessed to a request being in secure mode. (Column 12, lines 25 – Column 13, line 50)
- Displaying an image corresponding to the data, where displaying an image corresponding to the data is inherent to the functioning of a frame buffer.

England et al. fails to disclose :

- Occluding the image prior to a platform transitioning out of isolated execution mode.

Cunnif et al. (Column 2, lines 40-45) & (Column 5, lines 8-36) discloses a method of occluding a part of an image based on the mode of execution or a mode of the processor, and will occlude images in one mode, prior to switching to another mode.

England et al. (Column 12, lines 25 – Column 13, line 50) teaches that memory mapped IO devices such as a frame buffer should not have their information be read by untrusted software. It would have been obvious to one of ordinary skill in the art at the time of invention to occlude the image information in the frame buffer in order to prevent other non-secure software and access requests from accessing the information.

Conclusion

9. Any inquiry concerning this communication from the examiner should be directed to Thomas M Ho whose telephone number is (571)272-3835. The examiner can normally be reached on M-F from 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on **(571)272-3799**

The Examiner may also be reached through email through **Thomas.Ho6@uspto.gov**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

General Information/Receptionist	Telephone: 571-272-2100	Fax: 571-273-8300
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TMH

May 14th, 2007

GILBERTO BARRON JR
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